Claims

[c1] 1. A method of fabricating an optoelectronic package comprising:

(a) positioning an optical device within a window of a substrate active-side up and below a top substrate surface;

(b) filling the window with an optical polymer material;

(c) planarizing surfaces of the optical polymer material and the substrate;

(d) patterning waveguide material over the optical polymer material and the substrate to form an optical interconnection path and to form a mirror to reflect light from the optical device to the interconnection path; and

(e) forming a via to expose a bond pad of the optical device.

[c2] 2. The method of claim 1 further comprising patterning a protective metallization layer over the mirror.

[c3] 3. The method of claim 2 further comprising, after (d) and before (e), applying an insulating layer over the patterned waveguide material,

wherein (e) comprises forming the via through the insulating layer extending to the bond pad, and

further comprising (f) patterning an electrically conductive interconnection layer extending over the insulating layer and into the via.

[c4] 4. The method of claim 3 wherein (d) comprises applying a first layer of cladding material over the optical polymer material and the substrate, applying a layer of core material over the first layer of cladding material, applying a second layer of cladding material over the layer of core material, and patterning the first layer of cladding material, the layer of core material, and the second layer of cladding material to form an angle of about 45 degrees.

[c5] 5. The method of claim 3 further comprising, prior to (a), providing a substrate comprising a window metallization layer extending at least partially on a bottom surface of the window and the top substrate surface and wherein (a) comprises positioning the optical device so as to at least partially overly the window metallization layer.

[c6] 6. The method of claim 5 wherein the window comprises a tapered ramp

extending between the optical device and the portion of the top substrate surface underlying the window metalization layer.

[c7] 7. The method of claim 6 wherein the substrate comprises a shallow recess in the top substrate surface in which the window metallization layer is situated.

[c8] 8. The method of claim 7 wherein (c) further comprises removing excess window metallization material from the top substrate surface.

[c9] 9. The method of claim 5 wherein (a) comprises using a material comprising a solder.

[c10] 10. The method of claim 5 further comprising, prior to applying the insulating layer, patterning a microstrip reference plane over the waveguide material.

[c11] 11. The method of claim 10 wherein (e) comprises forming a plurality of vias with at least one via extending to the microstrip metalization layer and at least one via extending to a portion of the window metallization layer situated on the top substrate surface.

[c12] 12. The method of claim 5 further comprising providing a first stripline reference plane on the waveguide material, and further comprising patterning a second stripline reference plane over at least a portion of the electrically conductive interconnection layer.

[c13] 13. The method of claim 5 wherein (a) comprises providing a substrate comprising a first stripline reference plane patterned thereon, and further comprising patterning a second stripline reference plane over at least a portion of the electrically conductive interconnection layer.

[c14] 14. The method of claim 13 wherein (e) comprises forming a plurality of vias with at least one via extending to the first stripline reference plane and at least one via extending to a portion of the window metallization layer situated on the top substrate surface.

[c15] 15. The method of claim 3 further comprising removing at least a portion of the insulating layer extending over the mirror and the protective metallization layer,

and removing the protective metallization layer from the mirror.

[c16] 16. The method of claim 1 wherein (a) comprises positioning an electronic device within the at least one window of the substrate active-side up, wherein (e) comprises forming vias to expose bond pads of the electronic device, and further comprising (f) electronically interconnecting the exposed bond pads of the electronic and optical devices.

[c17] 17. The method of claim 16 further comprising, after (d) and before (e), applying an insulating layer over the patterned waveguide material, wherein (e) comprises forming the vias through the insulating layer extending to the bond pads, and wherein (f) comprises patterning an electrically conductive interconnection layer extending over the insulating layer and into the vias.

[c18] 18. The method of claim 17 further comprising attaching a heat sink to a surface of the substrate opposite the top substrate surface.

[c19] 19. The method of claim 18 wherein the electronic device comprises a multichip module.

[c20] 20. An optoelectronic package comprising:
(a) a substrate;
(b) an optical device positioned within a window of the substrate active-side up and below a top substrate surface;
(c) an optical polymer material surrounding the optical device within the window and having a planar surface with respect to the top substrate surface; and
(d) waveguide material patterned over the optical polymer material and the substrate and forming an optical interconnection path and a mirror configured for reflecting light from the optical device to the interconnection path, the waveguide having a via to expose a bond pad of the optical device.

[c21] 21. The package of claim 20 further comprising a protective metallization layer over the mirror.

[c22] 22. The package of claim 20 further comprising, an insulating layer over the patterned waveguide material, the insulating layer having the via extending

therethrough towards the bond pad, and an electrically conductive interconnection layer extending over the insulating layer and into the via.

[c23] 23. The package of claim 22 further comprising an opening in the insulating layer exposing at least a portion of the mirror.

[c24] 24. The package of claim 22 wherein the patterned waveguide material comprises a first layer of cladding material over the optical polymer material and the substrate, a layer of core material over the first layer of cladding material, and a second layer of cladding material over the layer of core material.

[c25] 25. The package of claim 22 wherein the substrate comprises a window metallization layer extending at least partially on a bottom surface of the window and the top substrate surface and wherein the optical device at least partially overlies the window metallization layer.

[c26] 26. The package of claim 25 wherein the window comprises a tapered ramp extending between the optical device and the portion of the top substrate surface underlying the window metalization layer.

[c27] 27. The package of claim 26 wherein the substrate comprises a shallow recess in the top substrate surface in which the window metallization layer is situated.

[c28] 28. The package of claim 25 further comprising a solder configured for coupling the optical device and the substrate.

[c29] 29. The package of claim 25 further comprising a microstrip reference plane over the waveguide material.

[c30] 30. The package of claim 29 wherein the insulating layer has a plurality of vias with at least one via extending to the microstrip reference plane and at least one via extending to a portion of the window metallization layer situated on the top substrate surface, and further comprising an electrically conductive interconnection layer overlying the insulating layer and electronically interconnecting the microstrip reference plane and the substrate window metallization layer.

[c31] 31. The package of claim 25 further comprising a first stripline reference plane on the waveguide material, and further comprising a second stripline reference plane over at least a portion of the electrically conductive interconnection layer.

[c32] 32. The package of claim 25 wherein (a) comprises a substrate comprising a first stripline reference plane patterned thereon, and further comprising a second stripline reference plane over at least a portion of the electrically conductive interconnection layer.

[c33] 33. The package of claim 32 wherein the insulating layer has a plurality of vias with at least one via extending to the first stripline reference plane and at least one via extending to a portion of the window metallization layer situated on the top substrate surface.

[c34] 34. The package of claim 20 further comprising an electronic device positioned within the at least one window of the substrate active-side up, and wherein the via comprises a plurality of vias, including vias exposing bond pads of the electronic device, and further comprising an electrically conductive interconnection layer overlying the insulating layer and electronically interconnecting the exposed bond pads of the electronic and optical devices.

[c35] 35. The package of claim 34 further comprising a heat sink attached to a surface of the substrate opposite the top substrate surface.

[c36] 36. The package of claim 35 wherein the electronic device comprises a multichip module.

[c37] 37. An optoelectronic package comprising:
(a) a substrate having windows;
(b) an optical device positioned within a first window of the substrate active-side up and below a top substrate surface;
(c) an electronic device positioned within a second window of the substrate active-side up and below the top substrate surface;
(d) an optical polymer material surrounding the optical device within the first window and having a planar surface with respect to the top substrate surface;
(e) filler material surrounding the electrical device within the second window

and having a planar surface with respect to the top substrate surface;
(f) waveguide material patterned over the optical polymer material, filler material, and the substrate and forming an optical interconnection path and a mirror configured for reflecting light from the optical device to the interconnection path;
(g) an insulating layer over the patterned waveguide material, the insulating layer and waveguide material having vias extending therethrough towards bond pads of the electrical and optical devices; and
(h) an electrically conductive interconnection layer extending over the insulating layer and into the vias.

[c38] 38. The package of claim 37 further comprising a protective metallization layer over the mirror.

[c39] 39. The package of claim 37 further comprising an opening in the insulating layer exposing at least a portion of the mirror.

[c40] 40. The package of claim 37 wherein the substrate comprises a window metallization layer extending at least partially on a bottom surface of the at least one window and the top substrate surface and wherein the optical device at least partially overlies the window metallization layer, wherein at least one of the vias extends to a portion of the window metallization layer situated on the top substrate surface.

[c41] 41. The package of claim 40 wherein the window comprises a tapered ramp extending between the optical device and the portion of the top substrate surface underlying the window metalization layer.

[c42] 42. The package of claim 41 wherein the substrate comprises a shallow recess in the top substrate surface in which the window metallization layer is situated.

[c43] 43. The package of claim 40 further comprising a microstrip reference plane over the waveguide material, wherein at least one of the vias extends to the microstrip reference plane.

[c44] 44. The package of claim 37 further comprising a heat sink attached to a

surface of the substrate opposite the top substrate surface.

[c45] 45. The package of claim 37 wherein the electronic device comprises a multichip module.

[c46] 46. An optoelectronic package comprising:
(a) a substrate having a window and comprising a window metallization layer extending at least partially on a bottom surface of the window and a top substrate surface;
(b) an optical device positioned within the window active-side up and below the top substrate surface at least partially overlying the window metallization layer;
(c) an optical polymer material surrounding the optical device within the window and having a planar surface with respect to the top substrate surface;
(d) waveguide material patterned over the optical polymer material and the substrate and forming an optical interconnection path and a mirror configured for reflecting light from the optical device to the interconnection path;
(e) a microstrip reference plane over the waveguide material;
(f) an insulating layer over the waveguide material and microstrip reference plane, the insulating layer and waveguide material having vias extending therethrough towards bond pads of the electrical and optical devices, the window metallization layer, and the microstrip reference plane; and
(g) an electrically conductive interconnection layer extending over the insulating layer and into the vias.

[c47] 47. The package of claim 46 further comprising a protective metallization layer over the mirror.

[c48] 48. The package of claim 46 further comprising an opening in the insulating layer exposing at least a portion of the mirror.

[c49] 49. The package of claim 46 further comprising a solder configured for coupling the optical device and the substrate.

[c50] 50. The package of claim 49 further comprising a heat sink attached to a surface of the substrate opposite the top substrate surface.

[c51] 51. The package of claim 46 wherein the window comprises a tapered ramp extending between the optical device and the portion of the top substrate surface underlying the window metalization layer.

[c52] 52. The package of claim 50 wherein the substrate comprises a shallow recess in the top substrate surface in which the window metallization layer is situated.

[c53] 53. An optoelectronic package comprising:
(a) a substrate having a window and comprising a window metallization layer extending at least partially on a bottom surface of the window and a top substrate surface and a first stripline reference plane patterned on the substrate;
(b) an optical device positioned within the window active-side up and below the top substrate surface at least partially overlying the window metallization layer;
(c) an optical polymer material surrounding the optical device within the window and having a planar surface with respect to the top substrate surface;
(d) waveguide material patterned over the optical polymer material and the substrate and forming an optical interconnection path and a mirror configured for reflecting light from the optical device to the interconnection path;
(e) an insulating layer over the waveguide material, the insulating layer and waveguide material having vias extending therethrough towards bond pads of the electrical and optical devices, the window metallization layer, and the first stripline reference plane;
(f) an electrically conductive interconnection layer extending over the insulating layer and into the vias; and
(g) a second stripline reference plane patterned over the waveguide material.

[c54] 54. The package of claim 53 further comprising a protective metallization layer over the mirror.

[c55] 55. The package of claim 53 further comprising an opening in the insulating layer exposing at least a portion of the mirror.

[c56] 56. The package of claim 53 further comprising a solder configured for coupling the optical device and the substrate.

[c57] 57. The package of claim 53 further comprising a heat sink attached to a surface of the substrate opposite the top substrate surface.

[c58] 58. The package of claim 53 wherein the window comprises a tapered ramp extending between the optical device and the portion of the top substrate surface underlying the window metalization layer.

[c59] 59. The package of claim 58 wherein the substrate comprises a shallow recess in the top substrate surface in which the window metallization layer is situated.

[c60] 60. An optoelectronic package comprising:

(a) a substrate having windows, a first window having a window metallization layer extending at least partially on a bottom surface of the first window and a top substrate surface;

(b) an optical device positioned within the first window active-side up and below the top substrate surface at least partially overlying the window metallization layer;

(c) a multichip module positioned within a second window of the substrate active-side up and below the top substrate surface;

(d) an optical polymer material surrounding the optical device within the first window and having a planar surface with respect to the top substrate surface;

(e) filler material surrounding the electrical device within the second window and having a planar surface with respect to the top substrate surface;

(f) waveguide material patterned over the optical polymer material, filler material, and the substrate and forming an optical interconnection path and a mirror configured for reflecting light from the optical device to the interconnection path;

(g) a microstrip reference plane over the waveguide material;

(h) an insulating layer over the patterned waveguide material and the microstrip reference plane, the insulating layer and waveguide material having vias extending therethrough towards bond pads of the multichip module and the optical device, the window metallization layer, and the microstrip reference plane; and

(i) an electrically conductive interconnection layer extending over the insulating

layer and into the vias.

[c61] 61. The package of claim 60 further comprising a protective metallization layer over the mirror.

[c62] 62. The package of claim 60 further comprising an opening in the insulating layer exposing at least a portion of the mirror.

[c63] 63. The package of claim 60 further comprising a heat sink attached to a surface of the substrate opposite the top substrate surface.

[c64] 64. The package of claim 60 further comprising a solder configured for coupling the optical device and the substrate.

[c65] 65. The package of claim 60 wherein the window comprises a tapered ramp extending between the optical device and the portion of the top substrate surface underlying the window metalization layer.

[c66] 66. The package of claim 65 wherein the substrate comprises a shallow recess in the top substrate surface in which the window metallization layer is situated.